



SAA7162E

PCI Express based dual channel multistandard audio and video decoder

Rev. 02 — 13 August 2007

Product short data sheet



1. General description

The SAA7162E is a dual channel multistandard audio and video TV decoder with digital IF demodulator and PCI Express interface. It provides 10-bit ADC, enhanced PAL/NTSC comb filtering, a versatile VBI data processing, more sophisticated scaling algorithms, support of high definition component video, picture improvement processing, more robustness with VCR type signals, increased audio functionality like SPDIF input/output, I²S-bus input/output and an integrated audio sample rate converter from 32 kHz to 44.1 kHz or 48 kHz.

The SAA7162E is a highly integrated circuit for e.g. TV insertion inside PC systems. The multistandard TV decoder covered all video color standards like PAL, NTSC and SECAM and sound standards like dual FM, NICAM, BTSC and EIAJ. Additional to the TV decoder function a digital IF demodulator, an FM radio decoder, standard interfaces for digital video and audio, remote control receiver and transmission processing and a high-speed programming port allows high integrated system solutions for multimedia application.

2. Features

2.1 Analog video acquisition

- Twenty analog inputs; allowing multiple combinations of
 - ◆ Dual channel CVBS
 - ◆ Dual channel S-video
 - ◆ Dual channel Y/C
 - ◆ One channel RGB or Y-P_B-P_R (progressive or interlaced); able to handle standard definition signals as well as HD0
 - ◆ Dual channel low IF from an NXP Silicon Tuner
- One channel RGB or Y-P_B-P_R component input according to
 - ◆ 480i and 576i (standard definition and interlaced)
 - ◆ 480p and 576p (HD0 and double scan rate) at two-fold over sampling (54 MHz)
- Software controlled gain adjustment for Y-P_B-P_R component inputs
- One channel 3-level input pins for one fully equipped D-terminal applications
- Eight video processing channels with automatic signal clamping and signal amplifying adjustment to a high quality 10-bit CMOS analog-to-digital converter results in a four-fold ITU-R BT.656 oversampled (54 MHz) video signal
- AGC for the selected CVBS or S-video channel, or manually adjustable gain for all video signal types

- Two channels with buffered analog outputs providing CVBS/S-video signal selected from any input
- Two channels with differential analog CVBS and SSIF outputs from the integrated digital video IF demodulator

2.2 Digital IF demodulator

- Two separate digital IF demodulators
 - ◆ Worldwide multistandard analog TV IF demodulator (M/N, B/G/H, D/K, I and L/L-accent standard)
 - ◆ FM radio pre-processing, internal selectivity for FM stereo application
 - ◆ Alignment-free application
 - ◆ Noise shaped IF AGC output signal
 - ◆ Easy programming of IF processing by TV or FM radio standard selection

2.3 Dual channel video signal processing and decoding

- Luminance and chrominance signal processing for PAL BGDHIN, combination PAL N, PAL M, NTSC M, NTSC Japan, NTSC 4.43 and SECAM
- High-performance super-adaptive NTSC/PAL comb filter for 2-dimensional chrominance/luminance separation for
 - ◆ Increased luminance and chrominance bandwidth for all NTSC and PAL standards
 - ◆ Reduced cross-color and cross luminance artefacts, even with critical color pattern
- Automatic detection of any supported color standard
- High-quality RGB and Y-P_B-P_R component processing for STV and progressive TV
- Optional reduced resolution for Y-P_B-P_R component processing of HDTV (1080i and 720p) sources
- Automatic detection of any supported video standard, including 480p, 576p, 720p and 1080i
- Automatic detection of signals from consumer grade sources (e.g. VTRs)
- Versatile BCS adjustment for CVBS/S-video, RGB and Y-P_B-P_R component processing
- Easy discrimination between CVBS and Y/C signals
- Digital PLL for synchronization and clock generation from all standards and non-standard video sources, e.g. consumer grade VTR
- Detection of copy protected input signals according to the Macrovision standard, indicating level of protection, including progressive signals 480p and 576p
- On-chip LLC generation according to ITU-R BT.601 (standard definition) or SMPTE 293M/ITU-R BT.1358 (HD0)

2.4 Dual channel video scalers

- Horizontal and vertical down-scaling and up-scaling to randomly sized windows
- Horizontal up-down scaling
 - ◆ Linear horizontal scaling ratio down to $\frac{1}{512}$ and up to 1024 limited by transfer data rates
 - ◆ Horizontal integer pre-scaler with range 1 to $\frac{1}{128}$
 - ◆ Horizontal VPD final scaler for down-scaling by $\frac{1}{7,999}$ to up-scaling by factor 1024

- Vertical up-down scaling
 - ◆ Linear phase accurate vertical scaling ratio down to 64 and up to 1024 limited by transfer data rates
 - ◆ Two separate 4-tap programmable polyphase filters for luminance (Y) and chrominance (U or V) data streams optimized for STV and HDTV
 - ◆ EDGI scale algorithm for areas with detected edges
 - ◆ Edge detector controlled mixing of 4-tap polyphase interpolator results and EDGI results enabling a maximum of performance with a minimize scale artefacts
- Two separated tasks processing pipes for active video (task A) and raw VBI (task B) regions
- Linear zooming of free programmable picture fragment
- Programmable panorama scaling
- Versatile BCS adjustment for scaled video outputs
- Optional DCI via programmable LUT
- Optional intrafield de-interlacing (EDGI)
- Optional CTI
- Optional RGB matrix and a programmable gamma correction

2.5 Dual channel advanced signal processing

- Support for letter box detection (black bar detection) via histogram evaluation
- Approximate noise level estimation of video input signal
- Status register and programmable status change output (interrupt) to minimize software overhead
- Support for RMS noise level estimation via histogram evaluation

2.6 Dual channel VBI slicing

- Versatile VBI data slicer (slicer, clock regeneration and data byte synchronization) for all common text and data services
 - ◆ WST525/WST625, Gemstar2x and Gemstar1x/VPS, VITC525/VITC625, CC525/CC625, WSS525 (CGMS)/WSS625, CGMS-A (line 41) of 480p (HD0), CGMS (line 41) of 576p (HD0), US NABTS/European teletext (FC) and MOJI (Japanese)
- Sliced VBI data can be transferred as ANC data on the digital video output ports (1, 2, 4 or 5) or on the parallel host port
- I²C-bus read-back access to data of following VBI data standards
 - ◆ Closed caption (CC525 and CC625), CGMS (WSS525), WSS625, Gemstar1x, Gemstar2x and VPS
- Optionally, raw data with dedicated gain and offset adjustment is available for software decoding

2.7 Digital peripheral interfaces

- Digital video input ports of 50 pins usable for maximum clock rates up to 75 MHz
 - ◆ Five independent standard TV (ITU-R BT.656 and VMI) 8-bit or 10-bit input streams
 - ◆ Two STV/HDTV 16-bit input streams
 - ◆ One STV/HDTV 20-bit input stream
 - ◆ One STV/HDTV 24-bit (RGB) input stream
 - ◆ Four TS or PS 8-bit input streams
- Selectable video input streaming standards
 - ◆ STV/HDTV video in ITU-R BT.656 representation, either 8-bit, 10-bit, 16-bit or 20-bit format $Y-C_B-C_R$ 4 : 2 : 2
 - ◆ STV/HDTV video in VMI representation, either 8-bit, 10-bit, 16-bit or 20-bit format
 - ◆ Optionally, STV/HDTV 24-bit (RGB) input stream converted to YUV 4 : 2 : 2 via internal programmable RGB/YUV matrix
- A digital video output port of 50 pins usable for maximum clock rates up to 75 MHz
 - ◆ Four independent TV streams [STV (ITU-R BT.656 (8-bit or 10-bit) or VMI (8-bit)) and STV/HDTV (16-bit)]
 - ◆ Four independent standard TV (ITU-R BT.656, VMI) 8-bit or 10-bit output streams
 - ◆ Two STV/HDTV 16-bit output streams
 - ◆ Two STV/HDTV 20-bit output streams
- Selectable video output streaming standards
 - ◆ STV/HDTV video in ITU-R BT.656 representation, either 8-bit, 10-bit, 16-bit or 20-bit format $Y-C_B-C_R$ 4 : 2 : 2, optional with included sliced VBI data and/or audio data
 - ◆ STV/HDTV video in VMI representation, either 8-bit, 10-bit, 16-bit or 20-bit format
- One serial input port for infrared transceivers supporting RC5 and RC6 transmission standards
- One serial output port for infrared transmitter adjustable to all common transmission standards

2.8 Analog audio acquisition

- Differential inputs of analog SSIF
 - ◆ Two differential SSIF signal inputs connectable to internal digital IF via simple post filter
 - or
 - ◆ Two single ended SSIF signal inputs connectable to conventional tuners (TV and FM)
- Sound processing channels with automatic signal clamping and signal amplifying adjustment to a high quality 10-bit CMOS ADC with 24.576 MHz sample frequency
- Three stereo analog audio baseband inputs with four serial sigma-delta 16-bit high resolution audio ADC
- Two stereo analog baseband outputs with filter stream stereo DACs
- Integrated analog audio pass-through (support for analog audio loopback cable to sound card)

2.9 TV sound decoder

- All standards TV stereo or mono sound decoder: BTSC, EIAJ, NICAM, FM A2 and AM
- dbx-TV noise reduction decoding for BTSC systems
- FM radio stereo decoding
- Automatic sound standard detection
- Automatic decoding for stereo and dual

2.10 Digital peripheral audio interfaces

- Two SPDIF inputs and two 24-bit SPDIF outputs (according to IEC 60958-3 and TTL compliant only) with 32 kHz, 44.1 kHz or 48 kHz
- Five I²S-bus inputs and two 24-bit I²S-bus outputs for up to 4 channels with 32 kHz, 44.1 kHz or 48 kHz
- Two inputs of external audio reference clock of $256 \times f_s$ or $384 \times f_s$
- Two outputs of audio output master clock ($512 \times f_s$, $256 \times f_s$ or $128 \times f_s$ selectable)
- Audio output sampling clock can be locked to video frame rate (constant number of audio samples per frame)

2.11 Audio feature processing

- Four stereo SRCs from 32 kHz, 44.1 kHz or 48 kHz to 32 kHz, 44.1 kHz or 48 kHz
- Volume, balance, bass and treble control
- Incredible Mono and Incredible Stereo
- AVL
- Optional generation of a frame locked audio master clock to support a constant number of audio clocks per video field

2.12 Programming ports

- PHI; byte oriented programming interface for fast access of modern microcontroller in future oriented PC TV applications
 - ◆ Fast alternative to I²C-bus based general control
 - ◆ Supports fast access to programming register (up to 8 MHz)
 - ◆ Supports 8-bit data and 16-bit address interface
 - ◆ Data read from VBI slicer (FIFO) for teletext decoding
 - ◆ IRQ register support
- Four I²C-bus interfaces
 - ◆ Support register access with 100 kHz and 400 kHz bit rate
 - ◆ I²C-bus master usable PHI port to program additional system devices like tuner, MPEG encoder and decoder
 - ◆ I²C-bus slave, usable to support a programming interface for application systems with limiting controller performance
 - ◆ Two 'silent' I²C-bus ports to support noise sensitive devices
- One SPI master interface for controlling external peripherals like MPEG encoder
- 28 GPIO pins, partly shared with interrupt and chip select functions

2.13 PCI Express interface

- Compliant to PCI Express Base Specification 1.0a
- The PCI Express circuit supports isochronous data traffic intended for uninterrupted transfer of streaming data like video streaming
 - ◆ x1 PCI Express endpoint (2.5 Gbit/s)
 - ◆ Data and clock recovery from serial stream
 - ◆ Low jitter and BER
- Type 0 configuration space header
 - ◆ 64-bit addressing
 - ◆ Single BAR; programmable address range of 17 bits, 18 bits, 19 bits or 20 bits dependent on application requirements
- PCI Express capabilities
 - ◆ 128 bytes write packet size and 64 bytes read packet size
 - ◆ MSI support
 - ◆ Software directed power management of four device power states (D0 to D3)
 - ◆ Active state power management of link states
 - ◆ Vendor specific capability for VC1 support; after reset VC1 isochronous capability is disabled

2.14 DMA support

- DMA write support
 - ◆ One DMA write channel for MSI
 - ◆ 12 DMA write channels for audio and video streaming: Maximum 8 software buffers per DMA channel or maximum buffer size of 2 MB
 - ◆ Round-robin arbitration between DMAs; support for graceful overflow recovery if PCI Express bandwidth is not provided in the required amount
- DMA read support
 - ◆ One DMA read channel for reading from page table(s); required for virtual-to-physical address translation of the streaming DMAs

2.15 General features

- Only a single crystal of 24.576 MHz or 32.11 MHz is required for all standards
- Software controlled power saving Standby modes
- Boundary scan test circuit according to 'IEEE Std. 1149.1'

3. Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------|--|---|------|-----|------|------|
| V _{DDDI0(1V8)_A} | digital internal supply voltage 0 (1.8 V) for unit A | | 1.65 | 1.8 | 1.95 | V |
| V _{DDDI3(1V8)_B} | digital internal supply voltage 3 (1.8 V) for unit B | | 1.65 | 1.8 | 1.95 | V |
| V _{DDDM0(1V8)_A} | memory digital supply voltage 0 (1.8 V) for unit A | | 1.65 | 1.8 | 1.95 | V |
| V _{DDDM0(1V8)_B} | memory digital supply voltage 0 (1.8 V) for unit B | | 1.65 | 1.8 | 1.95 | V |
| V _{DDDI1(1V2)} | digital internal supply voltage 1 (1.2 V) | | 1.1 | 1.2 | 1.3 | V |
| V _{DDDI2(1V2)} | digital internal supply voltage 2 (1.2 V) | | 1.1 | 1.2 | 1.3 | V |
| V _{DDD(PCI0)(1V2)} | PCI Express 0 digital supply voltage (1.2 V) | | 1.1 | 1.2 | 1.3 | V |
| V _{DDD(PCI1)(1V2)} | PCI Express 1 digital supply voltage (1.2 V) | | 1.1 | 1.2 | 1.3 | V |
| V _{DDDE0(3V3)_A} | digital extend supply voltage 0 (3.3 V) for unit A | | 3.0 | 3.3 | 3.6 | V |
| V _{DDDE2(3V3)} | digital extend supply voltage 2 (3.3 V) | | 3.0 | 3.3 | 3.6 | V |
| V _{DDDE3(3V3)} | digital extend supply voltage 3 (3.3 V) | | 3.0 | 3.3 | 3.6 | V |
| V _{DDDE4(3V3)} | digital extend supply voltage 4 (3.3 V) | | 3.0 | 3.3 | 3.6 | V |
| V _{DDDE5(3V3)} | digital extend supply voltage 5 (3.3 V) | | 3.0 | 3.3 | 3.6 | V |
| V _{DDDE6(3V3)_B} | digital extend supply voltage 6 (3.3 V) for unit B | | 3.0 | 3.3 | 3.6 | V |
| V _{DDD(PCI0)(1V0)} | PCI Express 0 digital supply voltage (1.0 V) | | 0.95 | 1.0 | 1.05 | V |
| V _{DDD(PCI1)(1V0)} | PCI Express 1 digital supply voltage (1.0 V) | | 0.95 | 1.0 | 1.05 | V |
| V _{DDA(DAC1_3V3)_A} | DAC 1 3.3 V analog supply voltage for unit A | | 3.1 | 3.3 | 3.5 | V |
| V _{DDA(DAC2_3V3)_A} | DAC 2 3.3 V analog supply voltage for unit A | | 3.1 | 3.3 | 3.5 | V |
| V _{DDA(PLL)(3V3)_A} | PLL analog supply voltage (3.3 V) for unit A | | 3.1 | 3.3 | 3.5 | V |
| V _{DDA0(3V3)_A} | analog supply voltage 0 (3.3 V) for unit A | | 3.1 | 3.3 | 3.5 | V |
| V _{DDA1(3V3)_A} | analog supply voltage 1 (3.3 V) for unit A | | 3.1 | 3.3 | 3.5 | V |
| V _{DDA2(3V3)_A} | analog supply voltage 2 (3.3 V) for unit A | | 3.1 | 3.3 | 3.5 | V |
| V _{DDA(ADC)(3V3)_A} | ADC analog supply voltage (3.3 V) for unit A | | 3.1 | 3.3 | 3.5 | V |
| V _{DDA(DAC1_3V3)_B} | DAC 1 3.3 V analog supply voltage for unit B | | 3.1 | 3.3 | 3.5 | V |
| V _{DDA(DAC2_3V3)_B} | DAC 2 3.3 V analog supply voltage for unit B | | 3.1 | 3.3 | 3.5 | V |
| V _{DDA(PLL)(3V3)_B} | PLL analog supply voltage (3.3 V) for unit B | | 3.1 | 3.3 | 3.5 | V |
| V _{DDA0(3V3)_B} | analog supply voltage 0 (3.3 V) for unit B | | 3.1 | 3.3 | 3.5 | V |
| V _{DDA1(3V3)_B} | analog supply voltage 1 (3.3 V) for unit B | | 3.1 | 3.3 | 3.5 | V |
| V _{DDA2(3V3)_B} | analog supply voltage 2 (3.3 V) for unit B | | 3.1 | 3.3 | 3.5 | V |
| V _{DDA(ADC)(3V3)_B} | ADC analog supply voltage (3.3 V) for unit B | | 3.1 | 3.3 | 3.5 | V |
| V _{DDA(PCI0)(3V3)} | PCI Express 0 analog supply voltage (3.3 V) | | 3.1 | 3.3 | 3.5 | V |
| V _{DDA(PCI1)(3V3)} | PCI Express 1 analog supply voltage (3.3 V) | | 3.1 | 3.3 | 3.5 | V |
| V _{DDA(1V8)_A} | analog supply voltage (1.8 V) for unit A | | 1.65 | 1.8 | 1.95 | V |
| V _{DDA(1V8)_B} | analog supply voltage (1.8 V) for unit B | | 1.65 | 1.8 | 1.95 | V |
| V _{DDA(OSC)(1V8)_A} | oscillator analog supply voltage (1.8 V) for unit A | | 1.65 | 1.8 | 1.95 | V |
| V _{DDA(OSC)(1V8)_B} | oscillator analog supply voltage (1.8 V) for unit B | | 1.65 | 1.8 | 1.95 | V |
| P _{tot} | total power dissipation | power management states; D0 for typical application | - | 3.7 | 4.2 | W |

Table 1. Quick reference data ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|------------------------------------|---|-----|-----|-----|--------|
| T _{amb} | ambient temperature | | 0 | - | 70 | °C |
| PCI Express link data rate | | | | | | |
| f _{RX} | receiver data rate | | - | 2.5 | - | Gbit/s |
| f _{TX} | transceiver data rate | | - | 2.5 | - | Gbit/s |
| 10-bit ADCs (including analog clamp and gain stages) | | | | | | |
| DLE _{DC} | DC differential linearity error | | - | 1 | - | LSB |
| ILE _{DC} | DC integral linearity error | | - | 1 | - | LSB |
| Analog video outputs (AVO_A1 and AVO_B1) | | | | | | |
| V _{o(p-p)} | peak-to-peak output voltage | for normal video levels 1 V (p-p); 75 Ω termination | - | 1 | - | V |
| 10-bit DACs (ASIFO_AP, ASIFO_AN, AVO_AP, AVO_AN, ASIFO_BP, ASIFO_BN, AVO_BP and AVO_BN) | | | | | | |
| DLE _{DC} | DC differential linearity error | | - | - | 1 | LSB |
| ILE _{DC} | DC integral linearity error | | - | - | 2 | LSB |
| Analog audio inputs (AAIL_AB2, AAIR_AB2, AAIL_A1, AAIR_A1) and analog audio outputs (AAOL_A2, AAOR_A2, AAOL_A1 and AAOR_A1) | | | | | | |
| V _{i(nom)(rms)} | nominal input voltage (RMS value) | | - | 200 | - | mV |
| V _{i(max)(rms)} | maximum input voltage (RMS value) | THD < 3 % | [1] | - | 1 | V |
| V _{o(nom)(rms)} | nominal output voltage (RMS value) | THD < 3 % | [2] | 180 | - | mV |
| V _{o(max)(rms)} | maximum output voltage (RMS value) | THD < 3 % | - | 1 | - | V |

[1] The analog audio inputs are supported by two input levels: 1 V (RMS) and 2 V (RMS), selectable independently per stereo input pair.

[2] Definition of levels and level setting:

- a) The full-scale level for analog audio signals is 0.8 V (RMS). The nominal level at the digital crossbar switch is defined at -15 dB (FS)
- b) Nominal audio input levels: external, mono, V_i = 180 mV (RMS); -15 dB (FS)

4. Ordering information

Table 2. Ordering information

| Type number | Package | | Version |
|-------------|---------|--|----------|
| | Name | Description | |
| SAA7162E | BGA756 | plastic ball grid array package; 756 balls; body 35 × 35 × 1.75 mm | SOT875-1 |

5. Block diagram

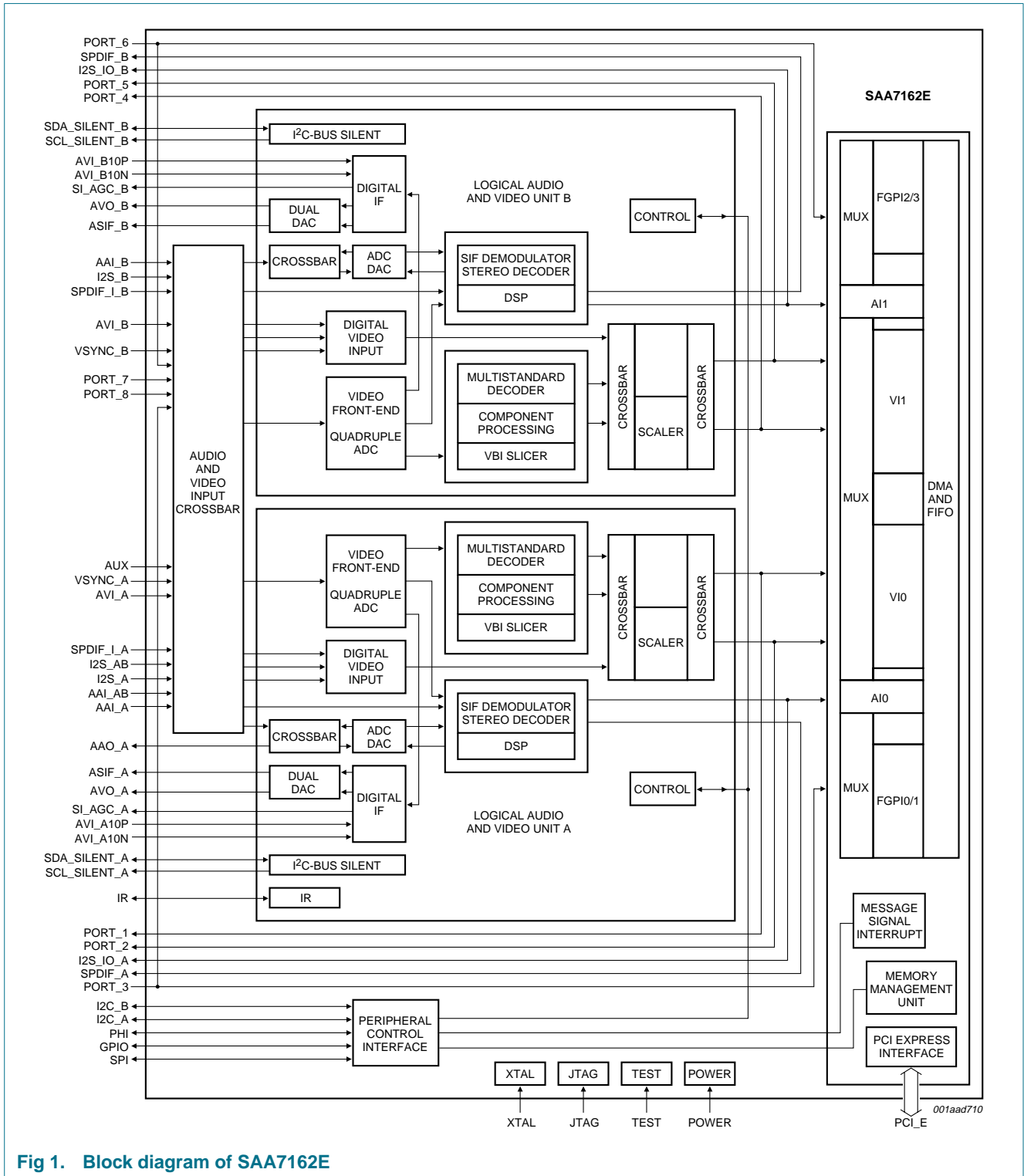


Fig 1. Block diagram of SAA7162E

6. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------------------|--|------------|------|-----------------------|------|
| V _{DDA(1V8)_A} | analog supply voltage (1.8 V) for unit A | | -0.5 | +2.5 | V |
| V _{DDA(1V8)_B} | analog supply voltage (1.8 V) for unit B | | -0.5 | +2.5 | V |
| V _{DDA(OSC)(1V8)_A} | oscillator analog supply voltage (1.8 V) for unit A | | -0.5 | +2.5 | V |
| V _{DDA(OSC)(1V8)_B} | oscillator analog supply voltage (1.8 V) for unit B | | -0.5 | +2.5 | V |
| V _{DDDI0(1V8)_A} | digital internal supply voltage 0 (1.8 V) for unit A | | -0.5 | +2.5 | V |
| V _{DDDI3(1V8)_B} | digital internal supply voltage 3 (1.8 V) for unit B | | -0.5 | +2.5 | V |
| V _{DDDM0(1V8)_A} | memory digital supply voltage 0 (1.8 V) for unit A | | -0.5 | +2.5 | V |
| V _{DDDM0(1V8)_B} | memory digital supply voltage 0 (1.8 V) for unit B | | -0.5 | +2.5 | V |
| V _{DDA(DAC1_3V3)_A} | DAC 1 3.3 V analog supply voltage for unit A | | -0.5 | +4.5 | V |
| V _{DDA(DAC2_3V3)_A} | DAC 2 3.3 V analog supply voltage for unit A | | -0.5 | +4.5 | V |
| V _{DDA(PLL)(3V3)_A} | PLL analog supply voltage (3.3 V) for unit A | | -0.5 | +4.5 | V |
| V _{DDA0(3V3)_A} | analog supply voltage 0 (3.3 V) for unit A | | -0.5 | +4.5 | V |
| V _{DDA1(3V3)_A} | analog supply voltage 1 (3.3 V) for unit A | | -0.5 | +4.5 | V |
| V _{DDA2(3V3)_A} | analog supply voltage 2 (3.3 V) for unit A | | -0.5 | +4.5 | V |
| V _{DDA(ADC)(3V3)_A} | ADC analog supply voltage (3.3 V) for unit A | | -0.5 | +4.5 | V |
| V _{DDA(DAC1_3V3)_B} | DAC 1 3.3 V analog supply voltage for unit B | | -0.5 | +4.5 | V |
| V _{DDA(DAC2_3V3)_B} | DAC 2 3.3 V analog supply voltage for unit B | | -0.5 | +4.5 | V |
| V _{DDA(PLL)(3V3)_B} | PLL analog supply voltage (3.3 V) for unit B | | -0.5 | +4.5 | V |
| V _{DDA0(3V3)_B} | analog supply voltage 0 (3.3 V) for unit B | | -0.5 | +4.5 | V |
| V _{DDA1(3V3)_B} | analog supply voltage 1 (3.3 V) for unit B | | -0.5 | +4.5 | V |
| V _{DDA2(3V3)_B} | analog supply voltage 2 (3.3 V) for unit B | | -0.5 | +4.5 | V |
| V _{DDA(ADC)(3V3)_B} | ADC analog supply voltage (3.3 V) for unit B | | -0.5 | +4.5 | V |
| V _{DDA(PCI0)(3V3)} | PCI Express 0 analog supply voltage (3.3 V) | | -0.5 | +4.5 | V |
| V _{DDA(PCI1)(3V3)} | PCI Express 1 analog supply voltage (3.3 V) | | -0.5 | +4.5 | V |
| V _{DDDE0(3V3)_A} | digital extend supply voltage 0 (3.3 V) for unit A | | -0.5 | +4.5 | V |
| V _{DDDE2(3V3)} | digital extend supply voltage 2 (3.3 V) | | -0.5 | +4.5 | V |
| V _{DDDE3(3V3)} | digital extend supply voltage 3 (3.3 V) | | -0.5 | +4.5 | V |
| V _{DDDE4(3V3)} | digital extend supply voltage 4 (3.3 V) | | -0.5 | +4.5 | V |
| V _{DDDE5(3V3)} | digital extend supply voltage 5 (3.3 V) | | -0.5 | +4.5 | V |
| V _{DDDE6(3V3)_B} | digital extend supply voltage 6 (3.3 V) for unit B | | -0.5 | +4.5 | V |
| V _{DDD(PCI0)(1V0)} | PCI Express 0 digital supply voltage (1.0 V) | | 0.85 | 1.15 | V |
| V _{DDD(PCI1)(1V0)} | PCI Express 1 digital supply voltage (1.0 V) | | 0.85 | 1.15 | V |
| V _{DDDI1(1V2)} | digital internal supply voltage 1 (1.2 V) | | -0.5 | +1.7 | V |
| V _{DDDI2(1V2)} | digital internal supply voltage 2 (1.2 V) | | -0.5 | +1.7 | V |
| V _{DDD(PCI0)(1V2)} | PCI Express 0 digital supply voltage (1.2 V) | | -0.5 | +1.7 | V |
| V _{DDD(PCI1)(1V2)} | PCI Express 1 digital supply voltage (1.2 V) | | -0.5 | +1.7 | V |
| V _i | input voltage | | -0.5 | V _{DD} + 0.5 | V |
| T _{stg} | storage temperature | | -40 | +125 | °C |

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|---------------------------------|--------------------------------------|-----|-------|------|
| T _{amb} | ambient temperature | | 0 | 70 | °C |
| V _{esd} | electrostatic discharge voltage | human body model [1] | - | ±2000 | V |
| | | machine model [2] | - | ±200 | V |

[1] Class 2 according to JESD22-A114-D.

[2] Class B according to EIA/JESD22-A115-A.

7. Package outline

BGA756: plastic ball grid array package; 756 balls; body 35 x 35 x 1.75 mm

SOT875-1

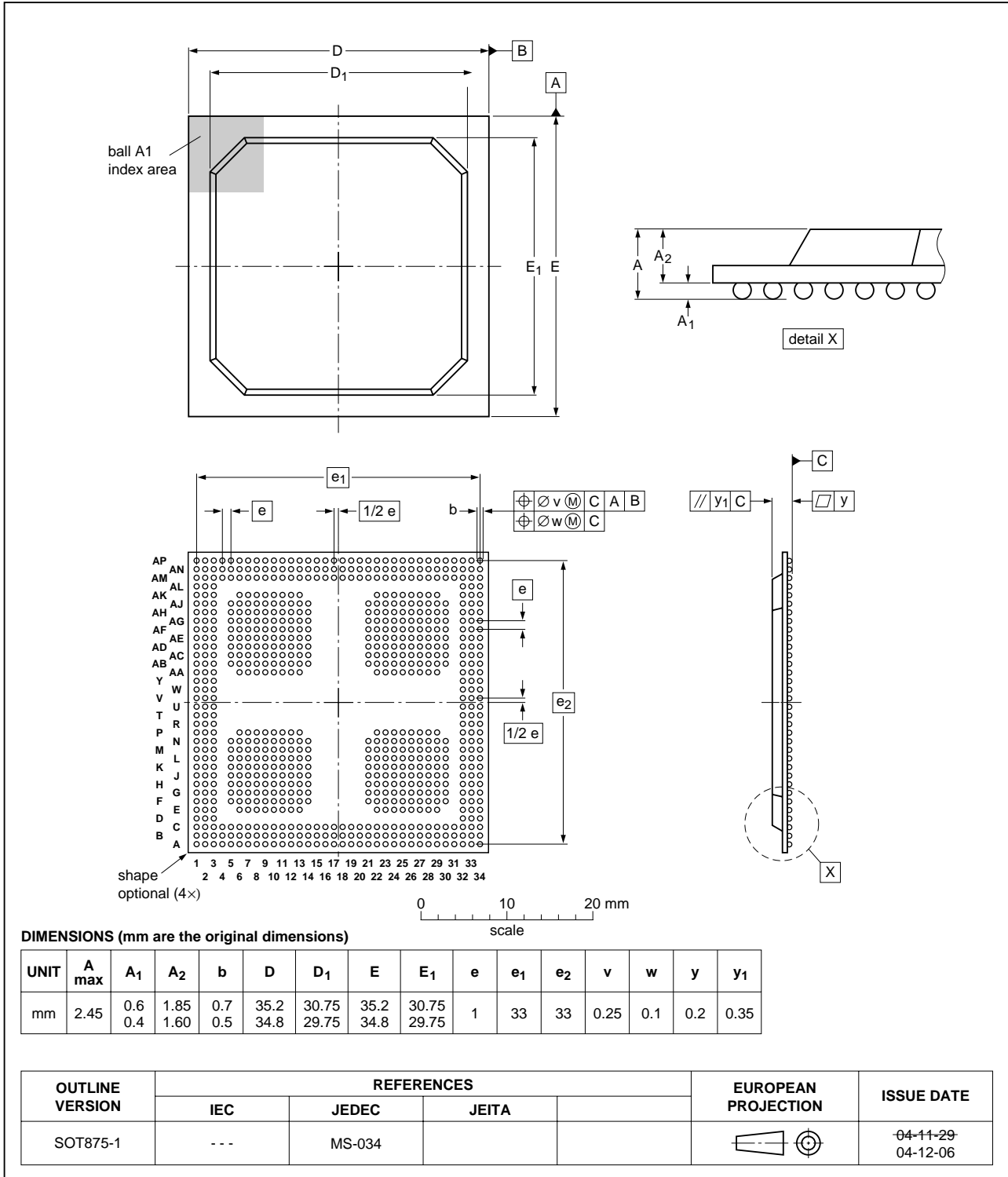


Fig 2. Package outline SOT875-1 (BGA756)

8. Abbreviations

Table 4. Abbreviations

| Acronym | Description |
|---------|--|
| ADC | Analog-to-Digital Converter |
| AGC | Automatic Gain Control |
| ANC | Ancillary |
| AVL | Automatic Volume Levelling |
| BAR | Base Address Register |
| BCS | Brightness Contrast Saturation |
| BER | Bit Error Rate |
| BTSC | Broadcast Television Systems Committee |
| CC | Closed Caption |
| CGMS | Copy Generation Management System |
| CMOS | Complementary Metal-Oxide Semiconductor |
| CTI | Color Transient Improvement |
| CVBS | Color Video Blanking Signal |
| DAC | Digital-to-Analog Converter |
| DC | Direct Current |
| DCI | Dynamic Contrast Improvement |
| DMA | Direct Memory Access |
| EDGI | Edge Guided 2-tap Interpolation |
| EIAJ | Electronic Industries Association/JEDEC standard |
| FC | Framing Code |
| FIFO | First In First Out |
| GPIO | General Purpose Input/Output |
| HD0 | High Definition 0 |
| HDTV | High Definition TV |
| IF | Intermediate Frequency |
| IRQ | Interrupt ReQuest |
| LLC | Line-Locked Clock |
| LUT | Look-Up Table |
| MPEG | Moving Picture Experts Group; the official name is ISO/IEC JTC1/SC29/WG11 (International Organization for Standardization/International Electrotechnical Commission, Joint Technical Committee 1, Subcommittee 29, Working Group 11) |
| MSI | Message Signal Interrupt |
| NABTS | North American Broadcast Text System |
| NICAM | Near Instantaneous Companded Audio Multiplex |
| NTSC | National Television Standards Committee |
| PAL | Phase Alternating Line |
| PC | Personal Computer |
| PCI | Peripheral Component Interconnect |
| PHI | Parallel Host port Interface |

Table 4. Abbreviations ...continued

| Acronym | Description |
|---------|---|
| PLL | Phase-Locked Loop |
| PS | Program Stream |
| RC | Remote Control |
| RGB | Red Green Blue |
| RMS | Root Mean Square |
| SECAM | Sequentiel Couleur avec Memoire |
| SPDIF | Sony Philips Digital Interface |
| SPI | Serial Peripheral Interface |
| SRC | Sample Rate Converter |
| SSIF | Second Sound Intermediate Frequency |
| STV | Standard TV |
| TS | Transport Stream |
| TTL | Transistor-Transistor Logic |
| VBI | Vertical Blanking Interval |
| VC | Virtual Channel |
| VCR | Voltage-Controlled Resistor |
| VITC | Vertical Interval Time Code |
| VMI | Video Module Interface |
| VPD | Variable Phase Delay |
| VPS | Video Programming System |
| VTR | Video Tape Recorder |
| WSS | Wide Screen Signalling |
| WST | World Standard Teletext |
| YUV | luminance (Y) and chrominance (U and V) |

9. Revision history

Table 5. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|---|------------------------------|---------------|----------------|
| SAA7162E_SDS_2 | 20070813 | Product short data sheet | - | SAA7162E_SDS_1 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. | | | |
| SAA7162E_SDS_1 | 20060710 | Preliminary short data sheet | - | - |

10. Legal information

10.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

10.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

10.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of

the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

10.4 Licenses

ICs with RC5 functionality

Purchase of an NXP Semiconductors IC with RC5 functionality does not convey an implied license under any trade secret, copyright, know-how or patent right to use this IC in any RC5 application. A license under applicable rights of Koninklijke Philips Electronics N.V. needs to be obtained via Philips Intellectual Property and Standards (www.ip.philips.com), e-mail: info.licensing@philips.com.

ICs with Macrovision copyright protection technology

This product incorporates copyright protection technology that is protected by method claims of certain U.S. patents and other intellectual property rights owned by Macrovision Corporation and other rights owners. Use of this copyright protection technology must be authorized by Macrovision Corporation and is intended for home and other limited viewing uses only, unless otherwise authorized by Macrovision Corporation. Reverse engineering or disassembly is prohibited.

ICs with RC6 functionality

Purchase of an NXP Semiconductors IC with RC6 functionality does not convey an implied license under any trade secret, copyright, know-how or patent right to use this IC in any RC6 application. A license under applicable rights of Koninklijke Philips Electronics N.V. needs to be obtained via Philips Intellectual Property and Standards (www.ip.philips.com), e-mail: info.licensing@philips.com.

Purchase of NXP ICs with digital dbx-TV noise reduction functionality

Licensed Chips — Purchase of NXP Semiconductors ICs with digital dbx-TV noise reduction functionality for which on top of the IC price, the related THAT Corporation royalty payment is paid to NXP Semiconductors, includes a license from THAT Corporation to use the ICs in a BTSC decoding application.

Unlicensed Chips — Purchase of NXP Semiconductors ICs with digital dbx-TV noise reduction functionality for which on top of the IC price, no related THAT Corporation royalty payment is paid to NXP Semiconductors, is only permitted to parties who according to information supplied to NXP Semiconductors by THAT Corporation, have a BTSC set-maker license from THAT Corporation,
45 Summer street, Milford, Massachusetts 01757-1656, USA.

10.5 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP B.V.

Silicon Tuner — is a trademark of NXP B.V.

11. Contact information

For additional information, please visit: <http://www.nxp.com>

For sales office addresses, send an email to: salesaddresses@nxp.com

Notes

12. Contents

1 General description 1

2 Features 1

2.1 Analog video acquisition 1

2.2 Digital IF demodulator 2

2.3 Dual channel video signal processing and decoding 2

2.4 Dual channel video scalers 2

2.5 Dual channel advanced signal processing 3

2.6 Dual channel VBI slicing 3

2.7 Digital peripheral interfaces 4

2.8 Analog audio acquisition 4

2.9 TV sound decoder 5

2.10 Digital peripheral audio interfaces 5

2.11 Audio feature processing 5

2.12 Programming ports 5

2.13 PCI Express interface 6

2.14 DMA support 6

2.15 General features 6

3 Quick reference data 7

4 Ordering information 8

5 Block diagram 9

6 Limiting values 10

7 Package outline 12

8 Abbreviations 13

9 Revision history 14

10 Legal information 15

10.1 Data sheet status 15

10.2 Definitions 15

10.3 Disclaimers 15

10.4 Licenses 15

10.5 Trademarks 16

11 Contact information 16

12 Contents 18

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2007. **All rights reserved.**
 For more information, please visit: <http://www.nxp.com>
 For sales office addresses, please send an email to: salesaddresses@nxp.com
 Date of release: 13 August 2007
 Document identifier: SAA7162E_SDS_2